Claims

[c1] 1. A method for designing an integrated circuit having multiple voltage domains, comprising:
(a) generating a logical integrated circuit design from information contained in a high-level design file, said high-level design file defining global connection declarations and voltage domain connection declarations;
(b) synthesizing said logical integrated circuit design into a synthesized integrated circuit design based upon said logical integrated circuit design, information in a voltage domain definition file and a design constraint file;
(c) generating a noise model from said synthesized integrated circuit design based on information in said voltage domain definition file, a circuit level profile and a design constraint file; and
(d) simulating said noise model against constraints in said design constraint file and constraints in a circuit level profile file to determine if said synthesized integrated circuit design meets predetermined noise targets.

[c2] 2. The method of claim 1, wherein said voltage domain definition file contains attributes of each global connection declaration and each voltage domain connection

declaration defined in said high-level design file.

[c3] 3. The method of claim 2, wherein said attributes of said global domain connection declarations and attributes of said voltage domain connection declarations are each independently selected from the group of attributes consisting of global attributes, voltage island attributes, flatten level attributes, off chip supply attributes, supply header attributes, controlled from attributes, ground noise isolated attributes, VSS rail value attributes, VDD rail attributes, internal power bus tag attributes and noise suppression required attributes.

[c4] 4. The method of claim 1, wherein said preferred components file comprises components selected from the group of components consisting of power supply elements such as regulators, voltage translators, on-chip capacitors, direct-chip-attach noise filters, on-package components such as resistors, capacitors, inductors, ferrites, voltage regulators, and combinations thereof.

[c5] 5. The method of claim 1, wherein said design constraint file comprises for each global domain and for each voltage domain, specifications independently selected from the group consisting of power rail noise specifications, ground noise specifications, power bus droop specifications, ground bus droop specifications, operating fre-

quency specifications, voltage domain switching factor specifications and a clock cycle offset factor specifications.

[c6] 6. The method of claim 1, wherein said circuit level profile file includes for each circuit or each circuit class, a single cycle current switching profile which can be instantiated in the noise model as a current source, an AC noise generation and acceptance profile, and a parasitic component estimate.

[c7] 7. The method of claim 1, further including:
(e) analyzing results of said simulation of said noise model to determine if any voltage domain fails; and
(f) for each failing voltage domain, proposing one or more alternative changes in said synthesized integrated circuit design.

[c8] 8. The method of claim 7, further including:
(g) selecting one or more of said one or more alternative changes and repeating steps (a) through (f) one or more times.

[c9] 9. The method of claim 1, further including:
(h) performing a physical design from said synthesized integrated circuit design.

[c10] 10. The method of claim 9, wherein step (h) includes:

removing placement attributes of said synthesized integrated circuit design; and
implementing within voltage domain, voltage domain to voltage domain and voltage domain to voltage supply relationships described in synthesized integrated circuit design.

[c11] 11. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for designing an integrated circuit having multiple voltage domains, said method comprising the computer implemented steps of:
(a) generating a logical integrated circuit design from information contained in a high-level design file, said high-level design file defining global connection declarations and voltage domain connection declarations;
(b) synthesizing said logical integrated circuit design into a synthesized integrated circuit design based upon said logical integrated circuit design, information in a voltage domain definition file and a design constraint file;
(c) generating a noise model from said synthesized integrated circuit design based on information in said voltage domain definition file, a circuit level profile file and

optionally and a design constraint file; and
(d) simulating said noise model against constraints in said design constraint file and constraints in a circuit level profile file to determine if said synthesized integrated circuit design meets predetermined noise targets.

[c12] 12. The system of claim 11, wherein said voltage domain definition file contains attributes of each global connection declaration and each voltage domain connection declaration defined in said high-level design file.

[c13] 13. The system of claim 12, wherein said attributes of said global domain connection declarations and attributes of said voltage domain connection declarations are each independently selected from the group of attributes consisting of global attributes, voltage island attributes, flatten level attributes, off chip supply attributes, supply header attributes, controlled from attributes, ground noise isolated attributes, VSS rail value attributes, VDD rail attributes, internal power bus tag attributes and noise suppression required attributes.

[c14] 14. The system of claim 11, wherein said preferred components file comprises components selected from the group of components consisting of power supply elements such as regulators, voltage translators, on-chip capacitors, direct-chip-attach noise filters, on-package

components such as resistors, capacitors, inductors, ferrites, voltage regulators, and combinations thereof.

[c15] 15. The system of claim 11, wherein said design constraint file comprises for each global domain and for each voltage domain, specifications independently selected from the group consisting of power rail noise specifications, ground noise specifications, power bus droop specifications, ground bus droop specifications, operating frequency specification, voltage domain switching factor specifications and a clock cycle offset factor specifications.

[c16] 16. The system of claim 11, wherein said circuit level profile file includes for each circuit or each circuit class, a single cycle current switching profile which can be instantiated in the noise model as a current source, an AC noise generation and acceptance profile, and a parasitic component estimate.

[c17] 17. The system of claim 11, further including the method steps of:
(e) analyzing results of said simulation of said noise model to determine if any voltage domain fails; and
(f) proposing one or more alternative changes to said synthesized integrated circuit design for each failing voltage domain.

[c18] 18. The system of claim 17, further including the method steps of:
(g) selecting one or more of said one or more alternative changes and repeating steps (a) through (f) one or more times.

[c19] 19. The system of claim 11, further including the method steps of:
(h) performing a physical design from said synthesized integrated circuit design.

[c20] 20. The system of claim 19, wherein method step (h) includes:
(h) removing placement attributes of said synthesized integrated circuit design; and
implementing within voltage domain, voltage domain to voltage domain and voltage domain to voltage supply relationships described in synthesized integrated circuit design.